AMENDMENTS TO THE SPECIFICATION:

Please amend the paragraph beginning on page 12, line 18, as follows:

~~Fig.1 shows~~ Figs. 1a and 1b show a structure of an embodiment of the present invention.

Please amend the paragraph beginning on page 13, line 10, as follows:

~~Fig.9 shows~~ Figs. 9a, 9b and 9c show an illustrative structure of a four-phase clock generating circuit according to an embodiment of the present invention.

Please amend the paragraph beginning on page 13, line 14, as follows:

~~Fig.11 illustrates~~ Figs. 11a and 11b illustrate the operation of an interpolator of a four-phase clock multiplexer circuit according to an embodiment of the present invention.

Please amend the paragraph beginning on page 14, line 4, as follows:

Reference is made to the drawings for illustrating the embodiment of the present invention. A clock and data recovery circuit in accordance with the preferred embodiment of the present invention, shown in ~~Figs.1 and 2~~ Figs. 1a, 1b and 2, includes a phase shift circuit 10 which comprises a switch 110 for receiving plural clocks of respective different phases and outputting selectively a plural number of sets of paired clocks, and an interpolator 111 comprised of a plural number of interpolators 111 (INT1 to INT8), for receiving paired clocks output from the switch 110 and outputting output clocks the delay time of which is prescribed by the time obtained on dividing with a preset interior division ratio of the phase difference between the clock pairs. A clock and data recovery circuit in accordance with the preferred embodiment of the present invention further includes a plural number of latch circuits 102 (F/F1 to F/F8) for sampling input data with a rising edge or a falling edge of the clocks (CLK1 to CLK8) output from the plural interpolators, a counter 103 for up-counting or down-counting

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depending on whether the outputs of the plural latch circuits (F/F1 to F/F8) indicate up or down-counting, respectively, a filter 105 for time averaging the output of the counter 103 and a decoder 106 for decoding an output of the filter 105. The outline of the configuration and operation of the respective components are hereinafter explained.

Please amend the paragraph beginning on page 24, line 12, as follows:

Fig.7 shows a configuration for generating the multi-phase clocks, supplied to the phase shift circuit 101, using a multi-phase clock generating circuit 200 employing a multiplier interpolator (multi-phase clock multiplier circuit). The phase shift circuit 101 of [[Fig.1]] Fig. 1a is made up of a multi-phase clock generating circuit 200 and a rotary switch 110. The interpolators 111_1 to 111_n output clocks CLK1 to CLKn, where n = 8, these clocks being fed to the clock input terminals of the D-flip-flop 102 of [[Fig.1]] Fig. 1a (F/F1 to F/F8). In Fig.7, reference clock generated by a clock generating circuit, such as a quartz oscillator, is used as a clock 1.

Please amend the paragraph beginning on page 25, line 14, as follows:

[[Fig.9]] Fig. 9a shows an illustrative structure of the four-phase clock multiplier circuit 202_n when the multi-phase clock multiplier circuit is arranged as the four-phase clock multiplier circuit. The four-phase clock multiplexer circuits 202_1 to 202_n are of the same structure.

Please amend the paragraph beginning on page 26, line 21, as follows:

Fig.10 is a signal waveform diagram showing the timing operation of the four-phase clock multiplier circuit 202 shown in [[Fig.9]] Fig. 9a. The rising of a clock T21 is determined by the internal delay of the timing difference division circuit 208 as from the rising of the clock Q(n-1)1, the rising of a clock T22 is determined by the timing division of the timings of the rise

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of the clock Q(n-1)1 and the rise of the clock Q(n-1)2 by the timing difference division circuit 209 and by the internal delay, and the rising of a clock T23 is determined by the timing division of the timings of the rise of the clock Q(n-1)1 and the rise of the clock Q(n-1)2 by the timing difference division circuit 210 and by the internal delay. In similar manner, the rising of a clock T26 is determined by the timing division of the timings of the rise of the clock Q(n-1)3 and the rise of the clock (n-1)4 by the timing difference division circuit 213 and by the internal delay, the rising timing of a clock T27 is determined by the internal delay of the timing of the rise of the clock Q(n-1)4 in the timing difference division circuit 214 and the rising of a clock T28 is determined by the timing division of the timings of the rise of the clock Q(n-1)4 and the rise of the clock (n-1)1 by the timing difference division circuit 215 and by the internal delay.

Please amend the paragraph beginning on page 28, line 12, as follows:

[[Fig.11]] Figs. 11a and 11b schematically [[shows]] show the operating principle of the timing difference division circuits 208, and 209. The timing difference division circuits 208, 210, 212 and 214 (homo), receiving the same signals, output signals with an inherent delay time, whereas the timing difference division circuits 209, 211, 213 and 215 (hetero), receiving two inputs exhibiting the phase difference T, output signals which undergo transition with a delay time corresponding to the sum of the delay time proper to the timing difference division circuit and time T/2 corresponding to one half the phase difference T (halved phase difference T).

Please amend the paragraph beginning on page 31, line 22, as follows:

The pulse correction circuits 216 to 223 generate duty-25% eight-phase pulses P21 to P28, each phase of which is shifted by 45°from one another (see ~~Figs.9 and 10~~ Figs. 9a, 9b, 9c and 10).

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Please amend the paragraph beginning on page 32, line 1, as follows:

The multiplexer circuits 224 to 227 generate duty 50% four-phase pulses Qn1 to Qn4, each phase of which is shifted by 90°from one another(see ~~Figs.9 and 10~~ Figs. 9a, 9b, 9c and 10).

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